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SYSTEM AND METHOD FOR DETERMINING THE VALUE OF A MEMORY ELEMENT

BACKGROUND

[0001] In today's society, computers are ubiquitous. For example, computers may be found in grocery stores, automobiles, airplanes, watches, or other electronic devices. Often computers include a processor that executes various functions such as mathematical computations, running programs, and retrieving and storing information. A processor that retrieves and stores information may use a storage device such as a disk drive (e.g., hard disk) or memory. Generally, memory devices store information in binary form—i.e., 1s and 0s. This binary information may be stored by assigning differing voltage states to binary values. For example, a binary 0 may be assigned 0 volts, while a binary 1 may be assigned 5 volts. Traditionally, memory devices have been implemented using transistors configured to form logic gates that are able to store binary values. However, recent trends include memory devices implemented using an array of magnetic elements that are constructed using semiconductor processing techniques.

[0002] One embodiment of an array of magnetic memory elements may comprise individual magnetic memory elements formed by using two layers of magnetic material that have adjustable magnetic orientations. The magnetic materials may be formed with an insulating layer sandwiched between them. Because the magnetic materials are designed to be adjustable, the magnetic field for each material may be adjusted by applying electrical current in proximity to the material. The orientations of two magnetic layers may be in the same direction (termed "parallel"), or they may be opposite each other (termed "anti-parallel").

[0003] Each magnetic memory element may also have an electrical resistance. The electrical resistance of the magnetic memory element may vary depending on the parallel or anti-parallel orientation of the magnetic fields. For example, parallel orientation may yield a resistance of 1 MΩ whereas anti-parallel orientation may produce a resistance of 1.1 MΩ. Because the resistance of the magnetic memory element may be changed, binary values (e.g., 1s and 0s) may be associated with the electrical resistance. Circuitry may be used to estimate the resistive value of the memory elements, and consequently determine the memory element's digital value. For one or more reasons, estimations for the resistive value of an individual memory element within the memory array may be inaccurate, which may then cause the digital value to be inaccurately determined.

SUMMARY

[0004] In one exemplary embodiment, a method for determining the memory element values is disclosed. In some embodiments the method may include: selecting a column of interest containing a desired memory element, disabling the desired memory element, measuring a first current provided to the column of interest, adjusting measurement circuitry to compensate for skew introduced by undesired memory elements, enabling the desired memory elements, and measuring a second current provided to the column of interest.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] For a detailed description of the preferred embodiments of the invention, reference will now be made to the accompanying drawings in which:

[0006] Figure 1 shows a computer system in accordance with various embodiments;

[0007] Figure 2A shows a memory array in accordance with various embodiments;

[0008] Figure 2B shows selection of a desired memory element in accordance with various embodiments;

[0009] Figure 3 shows circuitry for reading a desired memory element in accordance with various embodiments; and

[0010] Figure 4 shows a method for determining the value of a desired memory element in accordance with various embodiments.

NOTATION AND NOMENCLATURE

[0011] Certain terms are used throughout the following description and claims to refer to particular system components. As one skilled in the art will appreciate, different companies may refer to a component by different names. This document does not intend to distinguish between components that differ in name but not function. In the following discussion and in the claims, the terms "including" and "comprising" are used in an open-ended fashion, and thus should be interpreted to mean "including, but not limited to..." Also, the term "couple" or "couples" is intended to mean either an indirect or direct electrical connection. Thus, if a first device couples to a second device, that connection may be through a direct electrical connection, or through an indirect electrical connection via other devices and connections.

[0012] The term "magneto-resistive element" is intended to refer to an element whose electrical resistance varies as a function of the magnetic field induced on the element.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0013] The following discussion is directed to various embodiments of the invention. Although one or more of these embodiments may be preferred, the embodiments disclosed should not be interpreted or otherwise used as limiting the scope of the disclosure, including the claims. In addition, one skilled in the art will understand that the following description has broad application, and the discussion of any embodiment is meant only to be exemplary, and is not intended to intimate that the scope of the disclosure, including the claims, is limited to these embodiments.

[0014] Figure 1 illustrates an exemplary computer system 100. The computer system of Figure 1 includes a central processing unit ("CPU") 102 that may be electrically coupled to a bridge logic device 106 via a CPU bus. The bridge logic device 106 is sometimes referred to as a "North bridge." The North bridge 106 electrically couples to a main memory array 104 by a memory bus, and may further electrically couple to a graphics controller 108 via an advanced graphics processor ("AGP") bus. Note that the main memory array 104 may include magnetic memory array utilizing the methods for determining memory element

values disclosed below. The North bridge 106 may couple CPU 102, memory 104, and graphics controller 108 to the other peripheral devices in the system through, for example, a primary expansion bus ("BUS A") such as a PCI bus or an EISA bus. Various components that operate using the bus protocol of BUS A may reside on this bus, such as an audio device 110, an IEEE 1394 interface device 112, and a network interface card ("NIC") 114. These components may be integrated onto the motherboard, as suggested by Figure 1, or they may be plugged into expansion slots 118 that are connected to BUS A. If other secondary expansion buses are provided in the computer system, another bridge logic device 119 may be used to electrically couple the primary expansion bus, BUS A, to a secondary expansion bus ("BUS B"). This bridge logic 119 is sometimes referred to as a "South bridge."

[0015] Figure 2A shows a schematic representation of magnetic memory array 210, which may be implemented in memory array 104. Memory array 210 may include magnetic memory elements 212. Memory elements 212 may be arranged in an array of columns C_0-C_{N-1} and rows R_0-R_{N-1}. Individual memory elements may be depicted as resistive elements interconnecting rows and columns as shown. For example, memory element "0.0" would represent the memory element that is located at the intersection of row R_0 and column C_0. Note that the magnetic memory elements may be modeled using a variety of devices such as capacitors, resistors, inductors, tunnel junctions in series with diodes, or other combinations of integrated circuit elements.

[0016] Accompanying circuitry 220A-D may write data to and read data from the memory elements 212. Digital values may be written in memory array 210 by setting the resistance of the memory elements 212, where various resistive values may be assigned to various digital values. For example, memory element 0.0 may contain a resistance of 1 MΩ for a digital '1' or 1.1 MΩ for a digital '0', although the resistances may vary as desired. In addition, each memory element may be capable of being set to several distinct resistive values so that there may be N distinct data values represented by each memory element for N distinct resistive states. For example, memory element 0.0 may be set to four distinct resistive values, such as 1.0MΩ, 1.1MΩ, 1.2MΩ, and 1.3MΩ, so that memory

element 0.0 may be able to represent four distinct digital values—e.g., 00, 01, 10, and 11, respectively.

[0017] In order to determine the digital value contained in a memory element, voltage sources may be coupled to the rows R and columns C of memory array 210, as shown in Figure 2B. Coupling voltage sources to the array as shown offers the ability to isolate desired memory elements from undesired memory elements, while also allowing the digital value of the desired memory element to be determined. For example, memory element 0.0 may be isolated and read by coupling voltage source V_Y to columns C_0-C_{N-1}, voltage source V_X to rows R_1-R_{N-1}, and ground to row R_0 as shown. A voltage equivalent to voltage source V_Y may be provided to column C_0 by read circuitry 222. If V_Y and V_X are equal, then memory elements 1.0 through N-1.0 may be isolated from memory element 0.0, which may have V_Y across it. With memory element 0.0 isolated from the other memory elements in the same column, the current supplied to column C_0 may represent the resistance of memory element 0.0, so that the digital value of memory element 0.0 may be determined by measuring the current in column C_0. In addition to providing voltage source V_Y to column C_0, read circuitry 222 may be used to measure the current supplied to column C_0. However, V_Y and V_X may not be equal to each other and therefore the current supplied to column C_0 may also represent current in undesired memory elements, such as memory elements 1.0 through N-1.0.

[0018] Figure 3 shows an exemplary implementation of read circuitry 222 coupled to one or more memory elements 223. Circuitry 222 may be included in accompanying circuitry 220A-D (Figures 2A and 2B). Referring to Figure 3, memory elements 223 may include a desired memory element (i.e., a memory element that is to be measured), as well as other undesired memory elements (i.e., memory elements that may impact the measurement of the desired memory element). The desired memory elements may be represented by resistance R_{MEM}, while the undesired memory elements may be represented by resistance R_{LEAK}. A gain stage 224 may have its negative input coupled to the memory elements 223, its positive input coupled to a predetermined voltage V_Y, and its output coupled to a controller 226, where the controller 226 forms a negative

feedback loop. Controller 226 may be used to vary the amount of current in the feedback loop, where gain stage 224 may determine the amount of current that controller 226 shall provide.

[0019] The undesired memory elements R_{LEAK} may have one terminal coupled to the negative terminal of gain stage 224, which may be at a voltage potential V_X' as indicated in Figure 3, and its other terminal coupled to voltage source V_X. The desired memory element may have one terminal coupled to the negative terminal of gain stage 224 and the other terminal coupled to a switch 230. The gain stage 224 may attempt to maintain equal potentials at its positive and negative input nodes—i.e., V_Y equal to V_X'. The switch 230 may couple the desired memory element R_{MEM} to ground or may couple the desired memory element R_{MEM} to some other known state, such as voltage source V_X or high a impedance state. A current source 228 may also be coupled between a voltage supply V_S and the controller 226.

[0020] With the gain stage 224 configured in a negative feedback arrangement as shown in Figure 3, a voltage of approximately equal to voltage source V_X, indicated by V_X', may be established at the negative input of the gain stage 224. The voltages present at the input terminals may not be equal for various reasons including input offset errors of the gain stage 224. In establishing V_x' at the negative node of gain stage 224, the controller 226 may moderate the current flowing from current source 228. The controller 226 may be a metal oxide semiconductor transistor ("MOSFET"). The amount of current necessary to establish V_X' at the negative input terminal may be designated as I_{SENSE}. Under normal memory operation, the switch 230 may couple the desired memory element R_{MEM} to ground. If V_X' and V_Y are equal to each other, the undesired memory elements R_{LEAK} may conduct a minimal amount of current (e.g., 1nA) and may therefore be isolated from the desired memory element R_{MEM}. In this manner, I_{SENSE} may be primarily provided to R_{MEM} and may indicate the resistance and digital value of the desired memory element R_{MEM}.

[0021] In some situations, it may be difficult to generate matching voltages for V_Y and V_X'. If, V_X' and V_Y are not equal, then a portion of I_{SENSE} may be provided to R_{LEAK}, and consequently the digital value of the desired memory element R_{MEM}

may be skewed by the undesired memory elements R_{LEAK}. Using switch 230, the amount of skew introduced by the undesired memory elements R_{LEAK} may be characterized and compensated for if necessary, so that I_{SENSE} may be used to accurately determine the digital value of R_{MEM}. Note that this compensation may be made prior to or after measurement of I_{SENSE}. For example, gain stage 224 may have its offset voltage adjusted to compensate for skew prior to measuring I_{SENSE}, or I_{SENSE} may be measured and a correction factor may be added or subtracted from I_{SENSE} to correct for the amount of skew. I_{SENSE} may be measured at the junction between the current source 228 and the switch 226, as indicated by I_{OUT}.

[0022] Additionally, read circuitry 222 may include detection circuitry (not specifically shown in Figure 3) that measures the difference in the magnitude of I_{SENSE} with switch 230 in various conducting states. For example, when switch 230 couples the desired memory element R_{MEM} to ground, the magnitude of I_{SENSE} may be 1.5 μA, with 1μA flowing in R_{LEAK} and 0.5μA flowing in R_{MEM}—i.e., R_{MEM} enabled. Alternatively, when switch 230 couples the desired memory element R_{MEM} to V_X, the magnitude of I_{SENSE} may be 1.01μA, with 1μA flowing in R_{LEAK} and 0.01μA flowing in R_{MEM}—i.e., R_{MEM} disabled. In this example, the detection circuitry may note a 0.49μA difference between the two values of I_{SENSE}. Consequently, this difference may be compared to a predetermined difference amount, and then may represent the digital value of R_{MEM}. For example, a digital '1' may be represented by a difference current measurement in the range of 0.45μA to 0.60μA, and therefore a 0.49μA difference may indicate a digital '1'.

[0023] In addition, read circuitry may monitor the current in the desired memory element and determine the derivative of the current while the desired memory element R_{MEM} is being switched. In this manner, the peak value of the derivative may indicate the digital value of R_{MEM}.

[0024] In at least some embodiments, the current in the undesired memory elements R_{LEAK} should be less than or equal to about five times the current in the desired memory elements R_{MEM}.

[0025] Figure 4 illustrates a possible method for determining the digital value of a desired memory element R_{MEM}. A column of interest, which may contain the

desired memory element R_{MEM}, may be selected from within the memory elements 212 by coupling a voltage V_Y to the appropriate columns of memory elements 212 as shown in block 500. This may include coupling read circuitry 222 to the column of interest containing the desired memory element R_{MEM}, where, read circuitry 222 may provide the voltage V_Y to the column of interest. Note that read circuitry 222 may measure the amount of current I_{SENSE} provided to the column of interest in order to determine the digital value of the desired memory element R_{MEM}. A row of interest, which may contain the desired memory element R_{MEM}, may be isolated from other rows by coupling voltages V_X (and thereby generating V_x'), to the rows which do not contain the desired memory element R_{MEM} as shown in block 502. Because voltage V_X' may not equal V_Y the undesired memory elements R_{LEAK} may conduct current and the current I_{SENSE} measured by the read circuitry 222 may not accurately reflect the digital value of the desired memory element R_{MEM}. Switch 230 may disable the desired memory element R_{MEM} by coupling it to V_X or to a high impedance state as shown in block 504.

[0026] With the desired memory element R_{MEM} coupled to voltage V_X or to a high impedance state, the desired memory element R_{MEM} may be isolated so that amount of current in the undesired memory elements R_{LEAK} may be characterized by measuring the current I_{SENSE} as shown in block 506. In block 508, the amount of skew introduced by the undesired memory elements R_{LEAK} may be compensated for by using various techniques—e.g., adjusting the input offset voltage of gain stage 224. As shown in Figure 3, gain stage 224 may include an external control line for making the input offset adjustment. The desired memory element R_{MEM} may be enabled by coupling it to ground using switch 230 as shown in block 510. With the desired memory element R_{MEM} enabled, read circuitry 222 may measure I_{SENSE} as shown in block 512. Measuring the current I_{SENSE} after the compensating for the current consumed by the undesired memory elements R_{LEAK} may allow the digital value of the desired memory element R_{MEM} to be accurately determined.

[0027] Note that the above discussion and Figures address the situation where V_X' may be at a lower potential than V_Y, and therefore the current in the undesired

memory elements R_{LEAK} may flow from the negative terminal of gain stage 224 to voltage source V_X. However, V_X' may be at a higher potential than V_Y, and therefore the current in the undesired memory elements R_{LEAK} may flow from V_X to the negative terminal of gain stage 224. Accordingly, the methods, memory systems, and circuitry described above for compensating for the current in the undesired memory elements R_{LEAK} may be used regardless of the direction of the current in the undesired memory elements R_{LEAK}.

[0028] The above discussion is meant to be illustrative of the principles and various embodiments of the present invention. Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. For example, the switch 230 may be implemented using a tri-state buffer. Accordingly, aspects of the embodiments may be combined together in various forms to achieve desirable results. It is intended that the following claims be interpreted to embrace all such variations and modifications.